AMENDMENTS TO THE CLAIMS

Please amend the claims follows:

1. (Currently Amended) An echo canceller, for an asymmetric communication system configured to download an input signal at a first data rate and to upload an output data signal at a second data rate different from the first data rate, comprising[ ]:

a delay line block including a plurality m of delay lines used in central office (CO) mode for delaying an ~~echo~~ input signal for a predetermined interval to generate a delay signal, wherein fewer than m among the m delay lines are used for delaying the input signal while the echo canceller operates in a remote terminal (RT) mode, wherein while the echo canceller operates in the central office (CO) mode the second data rate is greater than the first data rate;

a filter coefficient table block for sequentially shifting filter coefficients stored in a shift register, and for sequentially outputting a filter coefficient; and

a multiplication and accumulation block for multiplying and adding the delay signal of the delay line block by the filter coefficient output by the filter coefficient table block to generate an echo-cancelled output signal.

2. (Currently Amended) The echo canceller of claim 1, wherein the echo canceller is a finite impulse response (FIR) filter that calculates the correlativity between the [echo] input signal and an echo output signal to generate the filter coefficients.

3. (Currently Amended) The echo canceller of claim 1, wherein the shift register is used while the echo canceller operates in ~~a~~ the central office (CO) mode and while the echo canceller operates in [an]the remote terminal (RT) mode[of the asymmetric communication system].

4. (Currently Amended) The echo canceller of claim 1, wherein the filter coefficient output by the filter coefficient table block has a shift rate equal to the ratio of

the first data rate and the second data rate~~[of 1:4]~~.

5. (Currently Amended) The ~~[asymmetric communication system]~~ echo canceller of claim 1, wherein while operating in the central terminal (CO) mode the delay line block divides a line for inputting the ~~[echo]~~input signal into eight delay lines to delay the ~~[echo]~~input signal.

6. through 17. (CANCELLED)

18. (New) An echo canceller, for an asymmetric communication system having a downstream data rate and an upstream data rate different from the downstream data rate, comprising:

an input interface block for receiving input data at a first data rate while operating in a first mode and at a second data rate while operating in a second mode;

a sub FIFO block configured to shift the input data at the first rate in the first mode by downsampling and configured to shift the echo input data at the second rate in the second mode by upsampling;

a main FIFO block configured to shift the echo input data at the second rate while operating in the first mode and configured to shift the echo input data at the first rate while operating in the second mode; and

an input interface block for generating an echo output signal at the second rate while operating in the first mode and generating an echo output signal at the first rate while operating in the second mode.

19. (New) The echo canceller of claim 18, wherein the main FIFO block and the sub FIFO block delay the echo input signal by a predetermined interval to generate a delay signal.

20. (New) The echo canceller of claim 18, wherein the echo canceller further includes a multiplication and accumulation block for multiplying and adding the delay signal by a filter coefficient output by a filter coefficient table block to generate an echo-cancelled echo output signal.

21. (New) The echo canceller of claim 18, wherein the main FIFO block is a 128-depth FIFO and the sub FIFO block is a four-depth FIFO.

22. (New) The echo canceller of claim 18, wherein the echo canceller operates upon an echo-dominant channel among channels of the asymmetric communication system.

23. (New) The echo canceller of claim 24, wherein the echo canceller receives the delay of the echo-dominant channel from a digital signal processor (DSP).

24. (New) An echo canceller for generating an echo-cancelled output signal in an asymmetric communication system configured to download an input data signal at a first data rate and to upload an output data signal at a second data rate different from the first data rate, comprising:

a delay line block having a plurality m of delay lines used in central office (CO) mode for delaying an input signal for a predetermined interval to generate a delay signal, wherein fewer than m among the m delay lines are used for delaying the input signal while the echo canceller operates in a remote terminal (RT) mode, wherein while the echo canceller operates in the central office (CO) mode the second data rate is greater than the first data rate.

25. (New) The echo canceller of claim 24 further comprising:

a filter coefficient table block for sequentially shifting filter coefficients stored in a shift register, and for sequentially outputting a filter coefficient; and